AMENDMENTS TO THE SPECIFICATION

Replace the paragraph starting at Page 4, line 19 with the following replacement

paragraph:

Figure 2 is a block diagram illustrating a network node 30 having a processor 110, a

network interface 120 such as a host channel adapter (HCA), and a memory controller 130

configured for controlling access to system memory resources 48.

Replace the paragraph starting at Page 11, line 11 with the following replacement

paragraph:

Flow control is handled by the embedded processor 80 based on reception of information

from the embedded processor input queue 78: in particular, the flow control protocol according

to the InfiniBand Architecture Specification uses a credit-based flow control. The embedded

processor 80 generates link flow control packets using the link flow control packet construction

module 82, based on messages stored into the embedded processor input queue 78. The

embedded processor 80 writes the link flow control packet to external memory 48; the embedded

processor 80 then generates a WQE that includes the associated operation and a pointer

specifying the location of a flow control packet into the embedded processor virtual lane FIFO

52a. The link flow control packet can then be output, specifying a number of available credits

for another transmitting note node.

Amendment filed July 10, 2003

Replace the paragraph starting at Page 11, line 23 with the following replacement paragraph:

According to the disclosed embodiment, application operations or are suspended based on detecting a depletion of flow control credits for a prescribed virtual lane, enabling network congestion to the reduced without wasting processor resources or system memory. Hence, processor resources and system memory can be redirected to unaffected application resources, optimizing efficiency and in the network node.

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